BADRINATH SINGHAL

badrinath2602@gmail.com ⋄ [Personal Website](#)

EDUCATION

- **Indian Institute of Technology (IIT) Guwahati** — July 2014 - June 2018
  Bachelor of Technology — CPI: 8.36/10
  Department of **Electronics and Electrical Engineering**
  Minor in **Computer Science and Engineering**

PUBLICATIONS

- **Badrinath Singhal**, Chris Voster, Di Meng, Gargi Gupta, Laura Dunne, Mark Germaine, *"A Machine Learning Approach to Digital Contact Tracing"*, *Under Review*

- U. Upadhyay, **B. Singhal** and M. Singh, *"Spinal Stenosis Detection in MRI using Modular Coordinate Convolutional Attention Networks,"* 2019 International Joint Conference on Neural Networks (IJCNN), Budapest, Hungary, 2019, pp. 1-8, doi: 10.1109/IJCNN.2019.8852085.

- S. A. Huddedar, M. Kagliwal, **B. Singhal** and F. C. Rhee, *"Performance Analysis of a Novel IT2 FCM Algorithm,"* 2018 IEEE International Conference on Fuzzy Systems (FUZZ-IEEE), Rio de Janeiro, 2018, pp. 1-7, doi: 10.1109/FUZZ-IEEE.2018.8491457.

WORK EXPERIENCE

Senior Machine Learning Engineer — January 2023 - Present
Axera Tech, Tokyo, Japan

- Developing AI based Image Signal Processor algorithms such as image denoising and demosiacking.
- Developing various modules in an image processing pipeline for camera such as white balancing, color correction matrix for our products.

Machine Learning Scientist — March 2020 - December 2022
EmbodyMe, Tokyo, Japan

- Working on 3D face reconstruction and expression and movement transfer in real time. Simultaneously working on deployment of models on platforms like windows and macos.
- Implemented virtual background on Xpression Camera, to be released on next version this year.
- Developed 3D character support for Xpression Camera which let's user use anime characters.
- Prepared potential future directions of our product and organisation structure
- Launched paid feature and paid user rate is growing around 50% weekly.

AI Scientist — Oct 2018 - August 2020
Synapsica, Bangalore, India

- Developed Synapsica Spindle *(Product demo)* which is an AI reporting assistant for MRI Spine saving upto 80% of reporting time of radiologists.
- Used computer vision and deep learning techniques to identify vertebral levels measures patency of central canal and characterises of disc herniation and nerve root compression.
- Prepared results for clinical validation of Spindle in India.
- Worked closely with radiologists in defining problem statement, reading papers and tried multiple approaches to before finalising a method.

Student Mentor — Oct 2019 - December 2020
Data Structures and Algorithms Nanodegree, Udacity

- Teaching, assisting and mentoring students globally for Udacity AI Nanodegree program.

· Weekly monitoring their performance in courses and assignments and providing feedback
· Providing guidance and motivation to students for completing the course.

Computer Vision and Fuzzy Systems Lab - Research Intern   May 2017 - July 2017
Prof. Frank Chung-hun Rhee, Hanyang University, Seoul, South Korea

· Integrated *Multi-EIASC Algorithm* with *IT2 Fuzzy C-Means Clustering Algorithm* to give *Multi-IT2 Fuzzy C-Means Algorithm.*
· Instead of using the EIASC algorithm over each of the dimensions of pattern sets separately, we used Multi-EIASC algorithm for the complete pattern set which uses n-dimensionality of pattern sets as its fundamental property.
· Our work got published in **IEEE WCCI 2018 at Rio, Brazil**.

PROJECTS

- **Detection of Spinal Stenosis from axial MRI scans.**
  Synapsica

  – Developed a deep learning and computer vision based 2 stage architecture which measures spinal canal diameter in axial image of MRI scan.

  – Perform training and testing on 9,000 MRI axial scans and tweaked model to improve performance of the model

  – **Our work got published at IEEE IJCNN 2019.**

- **Efficient VLSI Implementation of SVD**
  Bachelor Thesis Project
  Prof. Shaikh Rafi Ahmed, Dept. of EEE, IIT Guwahati

  – Used CORDIC algorithm to calculate the SVD of $n \times n$ matrix $(n > 2)$ using approach proposed to calculate SVD of 2×2 matrix using operations that can be implemented in VLSI architecture.

  – Involved reading papers, implementing and tested the approach on Verilog. Achieved reduction in processing time by 2% to calculate SVD.

TECHNICAL STRENGTHS

- **Programming Languages (or Libraries):** C/C++, Python, OpenCV, Matlab, Git, Docker, LaTeX, Pytorch, ONNX, CoreML, MC-Stan, Swift

- **Miscellaneous:** Simulink, ROS

ACADEMIC ACHIEVEMENTS

- Joint Entrance Examination Advanced 2014: Secured position in top 1% in India among 150000 students.

- Department rank 3 after freshman year at IIT Guwahati

- 5th Rank in Guwahati region for AISSCE 2013.

- Offered Merit cum Means (McM) scholarship by IIT Guwahati for 3 consecutive years till 2018.

- Among top 0.1% in India rank out of 1.5 million students in JEE Mains 2014.